HWT

Hardware Trace Framework

- Intel PT
- ARM Coresight
- ARM SPE

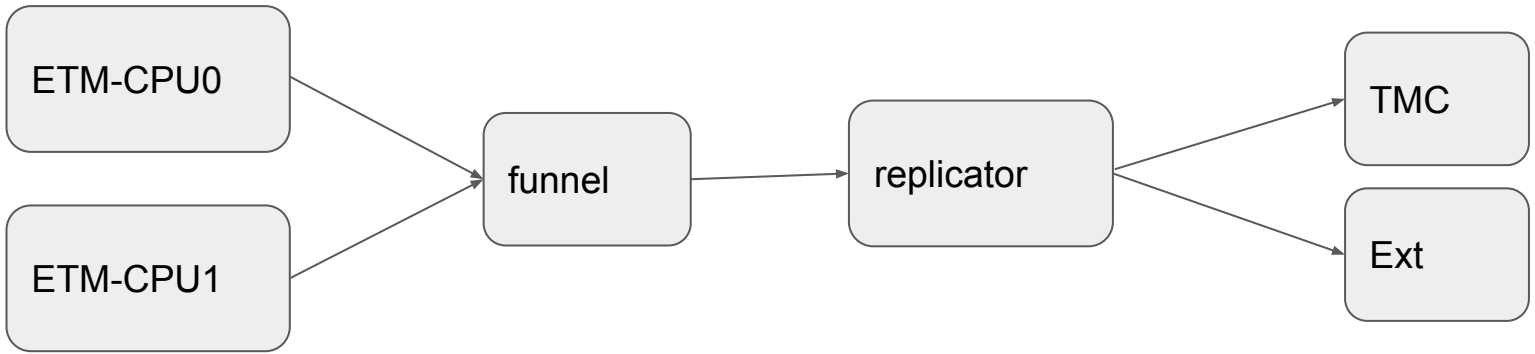
principle

Store events into DRAM

- Power events
- Branches, 1 bit
- Control flow changes
- Interrupts
- timestamps
- …

ARM Coresight

- Weird pipeline
- SoC-400 has bugs
- Memory mapped
- sys/arm64/coresight



Intel PT

Solid design

CPU instruction -based

Kernel support

- 3.5k lines of code
- Kernel hooks for sched/mmap
- ioctl-based trace context management
- /dev/hwt*
- Multiple backends support

```
Struct hwt_context {
    …
    int mode;
    struct hwt_owner *owner;
    LIST_HEAD *hwt_threads;
    LIST_HEAD *hwt_records;
    struct hwt_backend
    …
}
```

Instrumentation

hwt(1):

- Choose mode of operation
- Setup address range filtering
- Decoder libraries
- Process management
- Symbol lookup
- pause

Status

ARM Coresight – Fully functional

Intel PT – snippets available

SPE - work in progress by ARM Ltd

demo time

https://reviews.freebsd.org/D40466